

FIG. 1

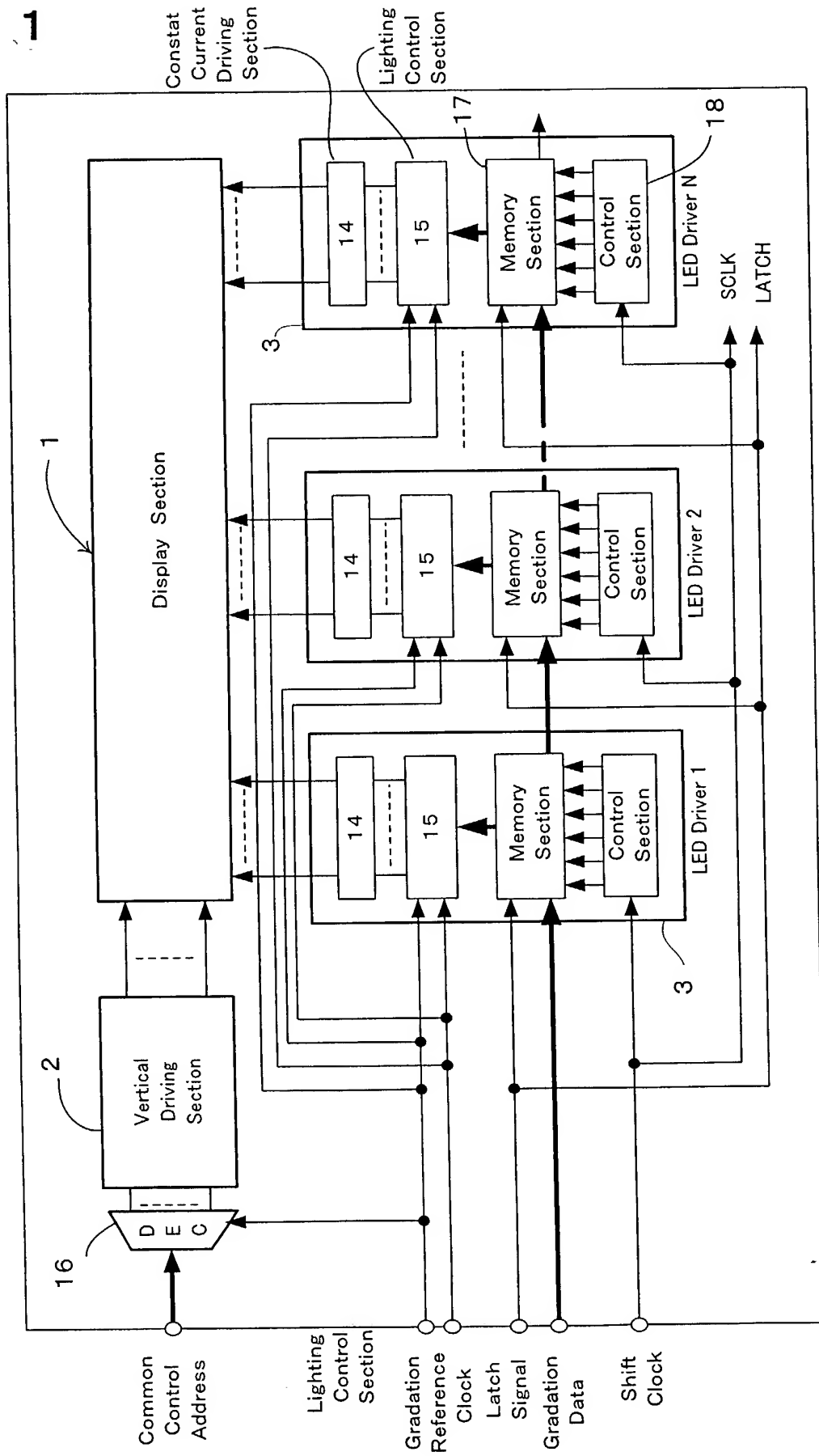
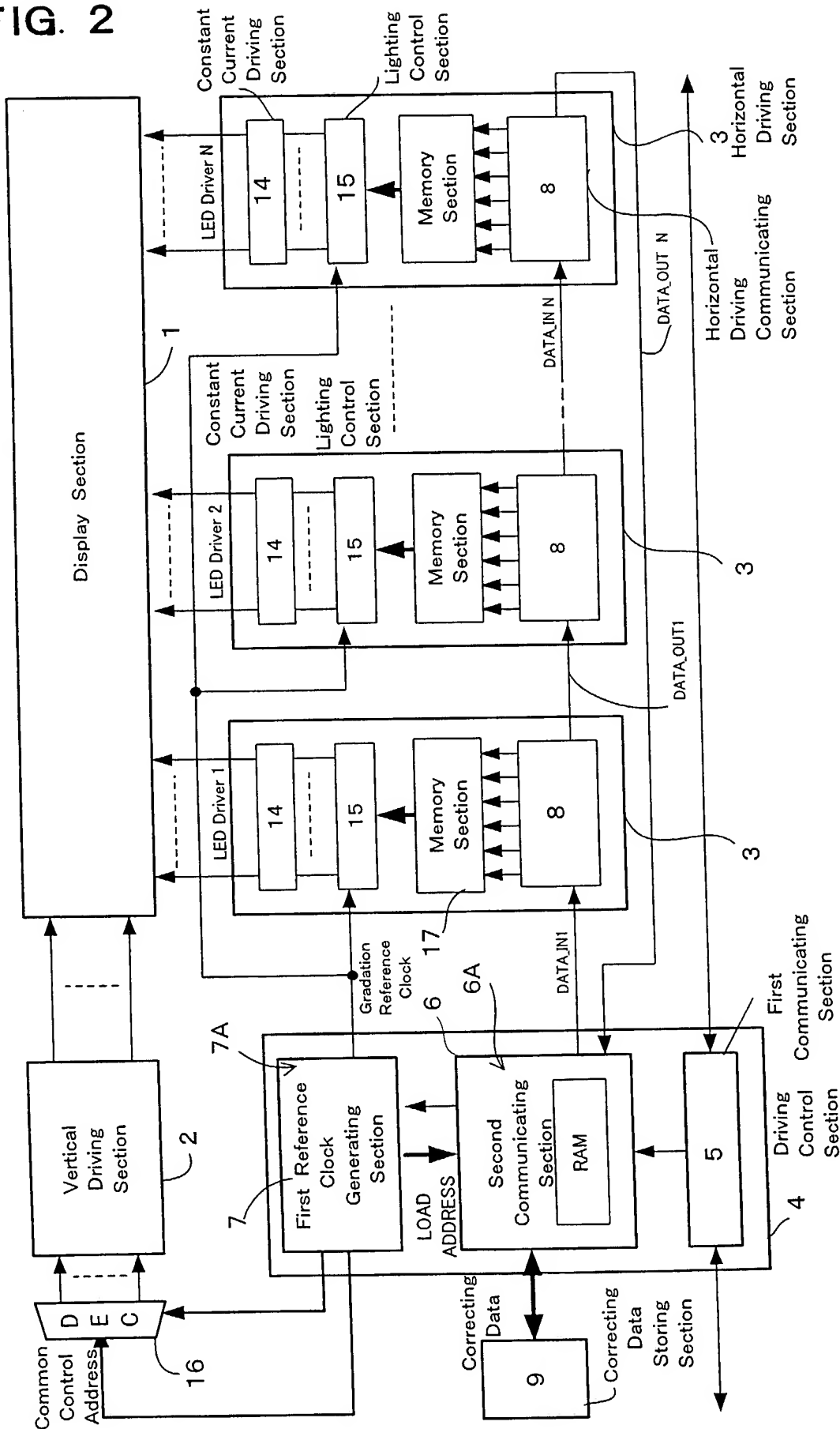


FIG. 2



The diagram illustrates the timing of various signals during a Quad-Speed lighting period. The top horizontal axis represents the 'Vsync: Frame Packet Period' and is divided into segments labeled 'csp', 'ud1', 'ud2', 'ud3', 'ud4', 'udN', 'csp', and 'res'. Below this, a 'vsync' signal is shown as a series of pulses. The 'Light Control Signal (BLANK)' is shown as a high-level signal. The 'Common Control Address' is shown as a sequence of addresses: 'adr\_0', 'adr\_1', 'adr\_2', 'adr\_3', 'adr\_0', 'adr\_1', 'adr\_2', 'adr\_3', 'adr\_0', 'adr\_1', 'adr\_2', 'adr\_3', 'adr\_0', 'adr\_1', 'adr\_2', 'adr\_3'. The 'Data DMA Control Section' is shown as a sequence of data: 'data\_0', 'data\_1', 'data\_2', 'data\_3', 'data\_0', 'data\_1', 'data\_2', 'data\_3', 'data\_0', 'data\_1', 'data\_2', 'data\_3', 'data\_0', 'data\_1', 'data\_2', 'data\_3'. The 'Control Section' is shown as a sequence of control signals: 'Hsync', 'drv1\_data', 'drv2\_data', 'drv3\_data', 'drv4\_data'. The 'BLANK' signal is shown as a high-level signal. The 'Common Control Address' is shown as a sequence of addresses: 'adr\_3', 'adr\_0'.

FIG. 4

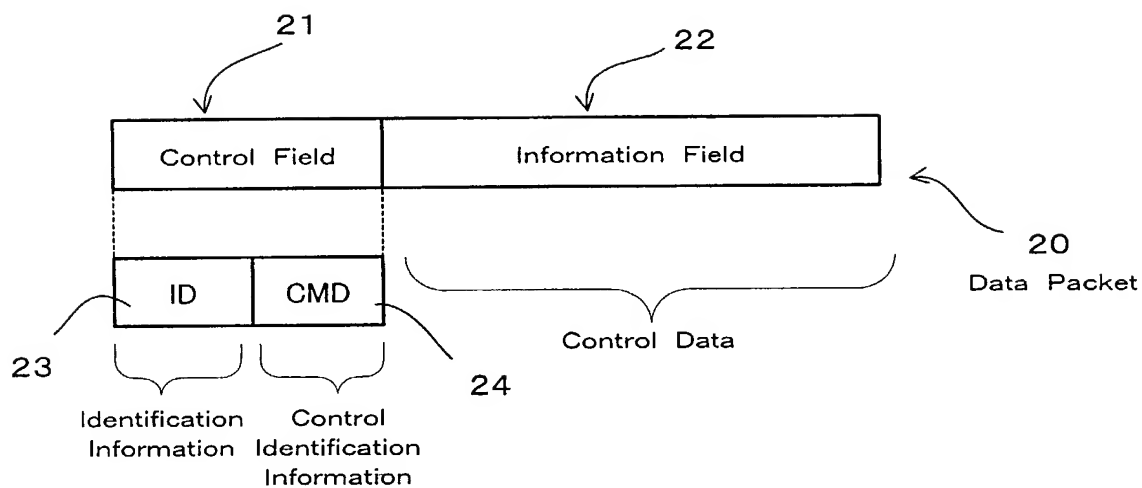


FIG. 5

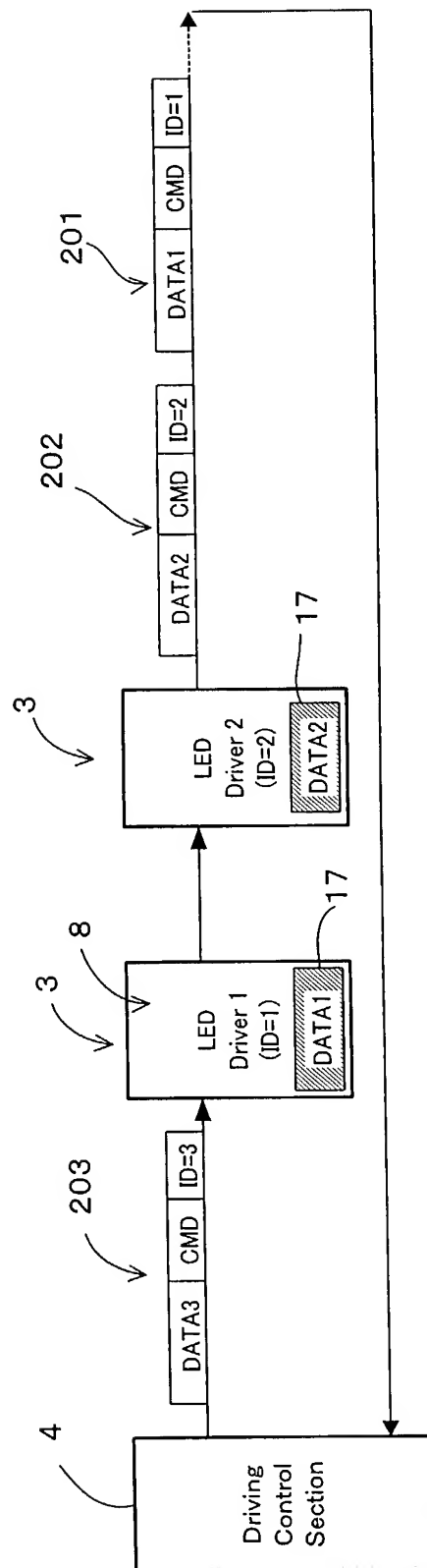


FIG. 6

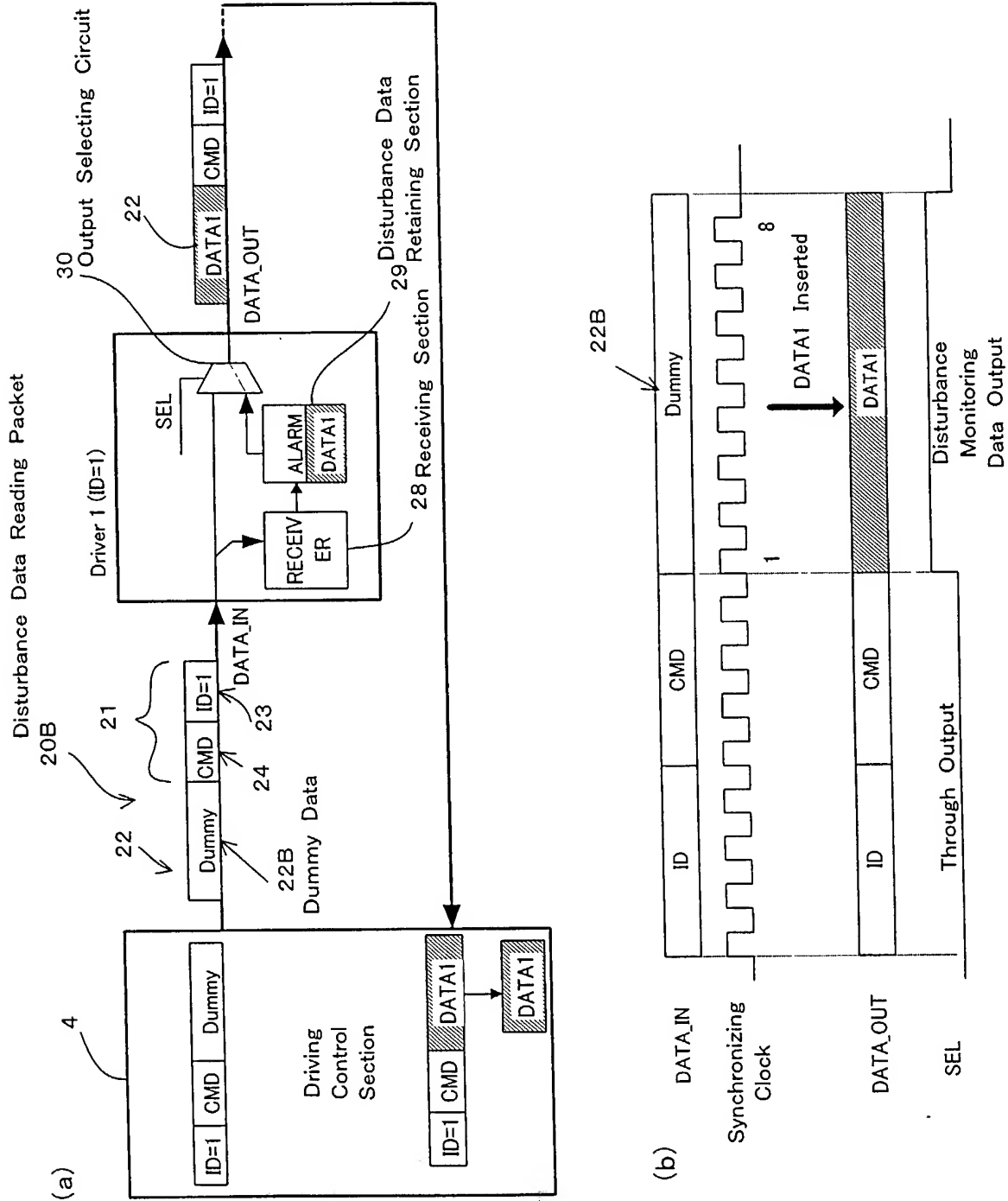
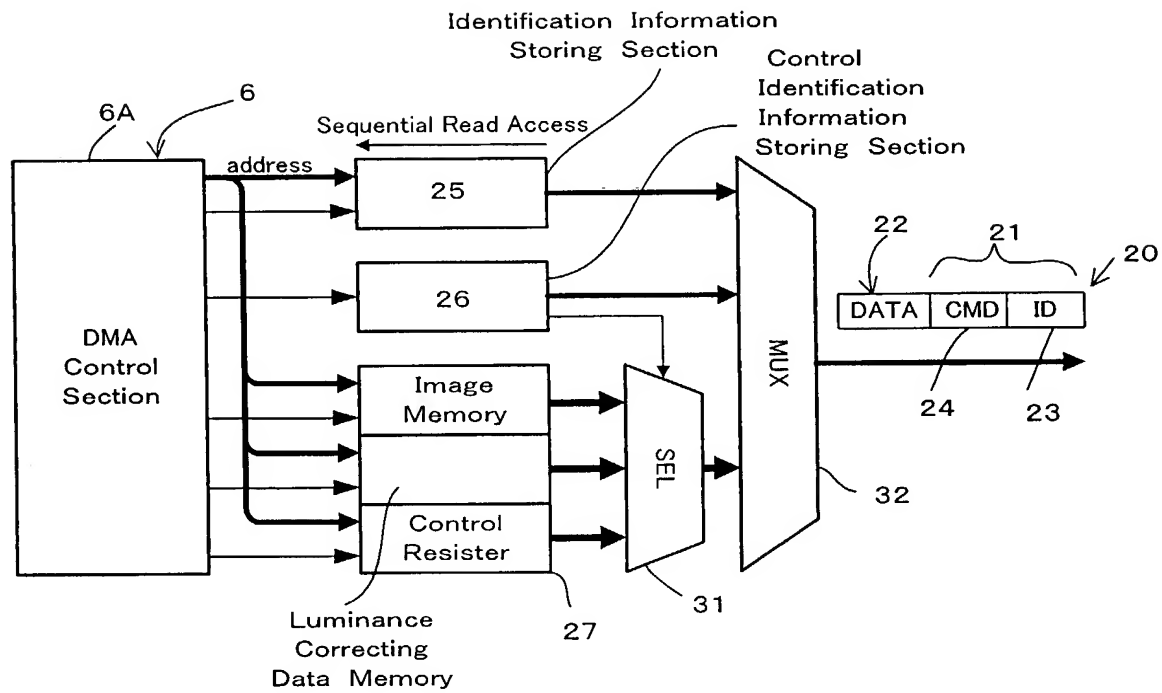
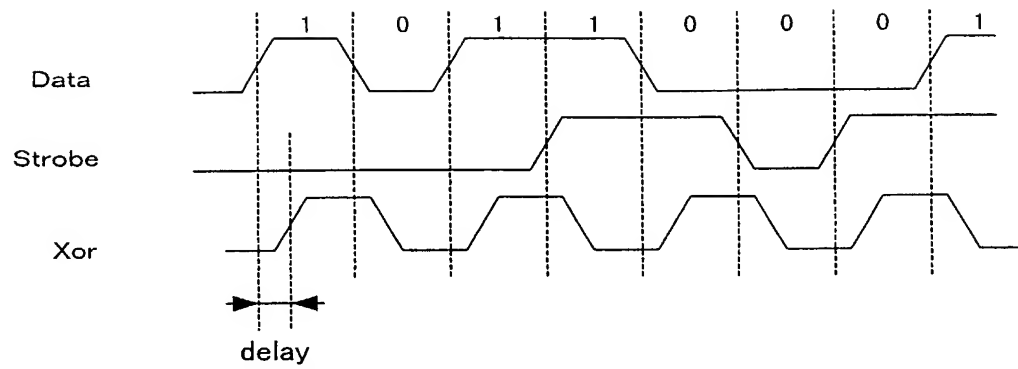
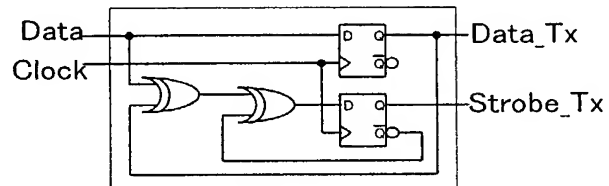


FIG. 7



**FIG. 8** (a)

(b)



(c)

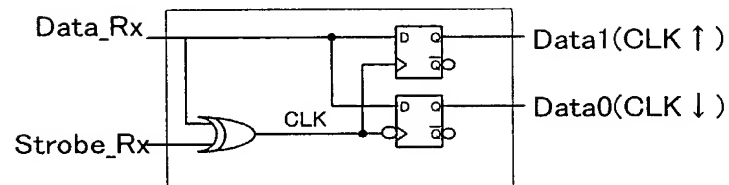




FIG. 9

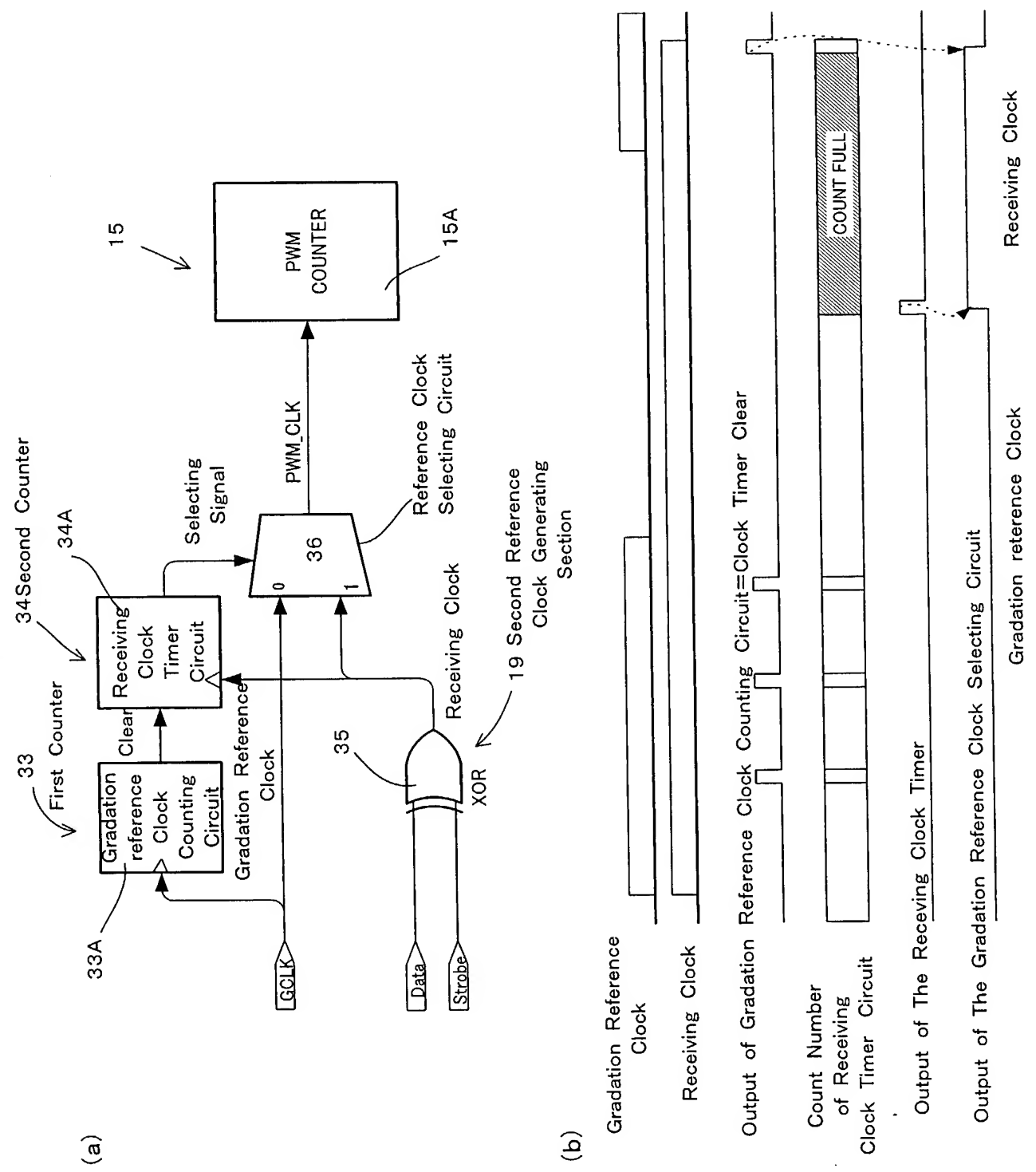


FIG. 10

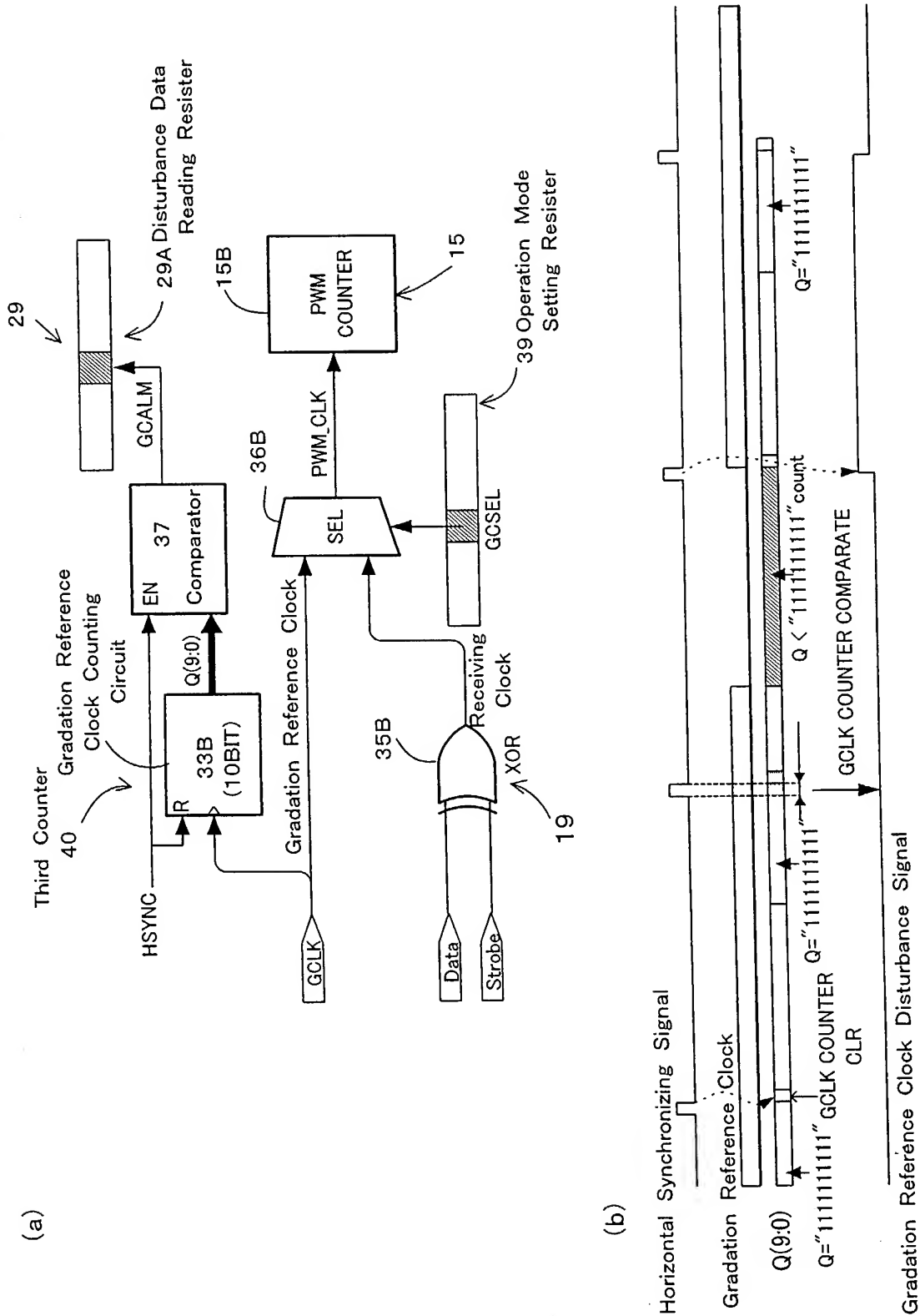
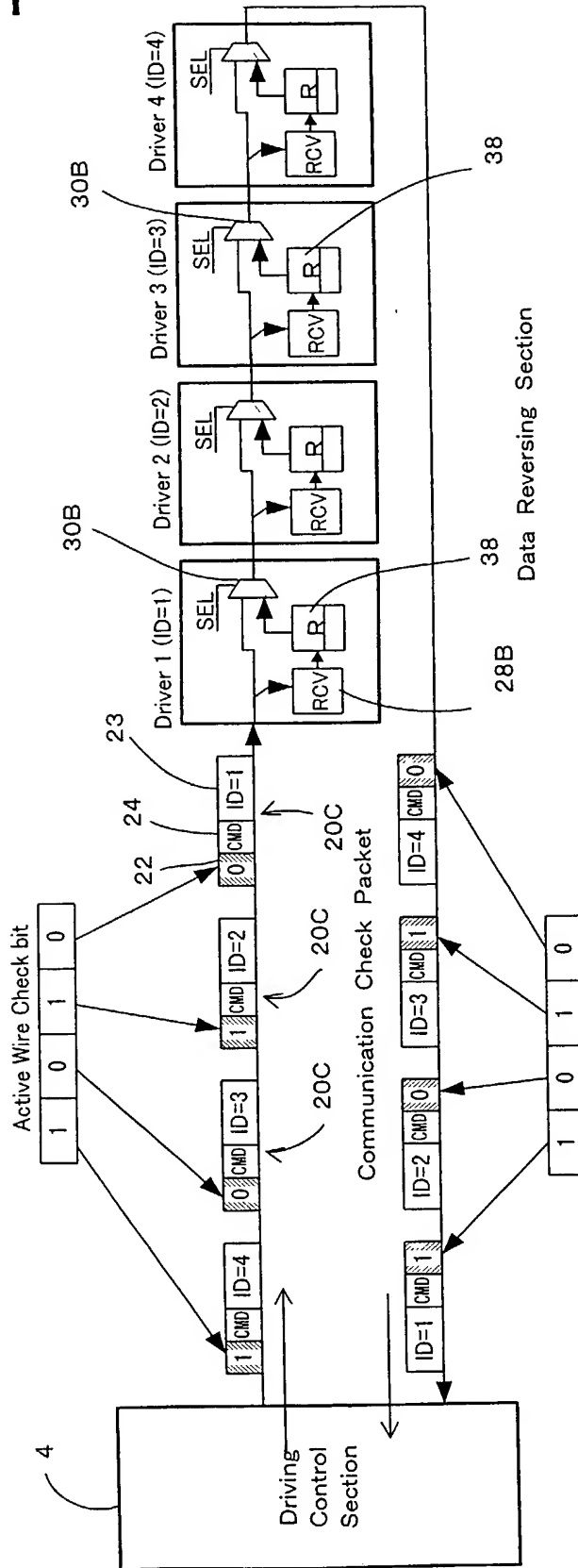


FIG. 11

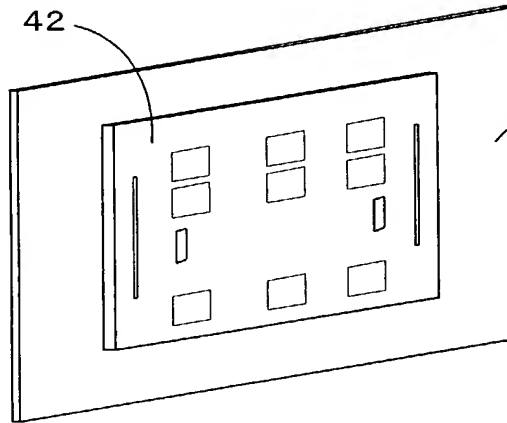


**FIG. 12**

(a)

Driving Circuit Board

42

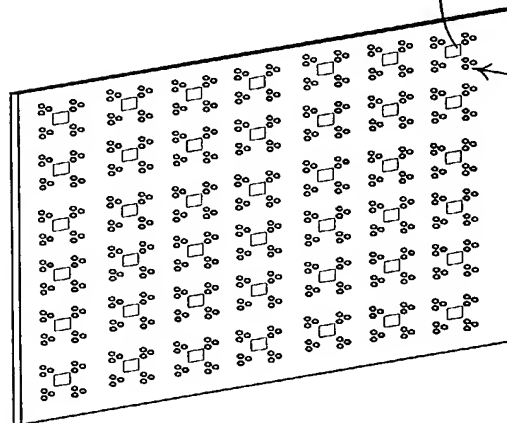


41

Lighting  
Element Board

(b)

Driving Circuit 10

Lighting Element  
11

46

FIG. 13

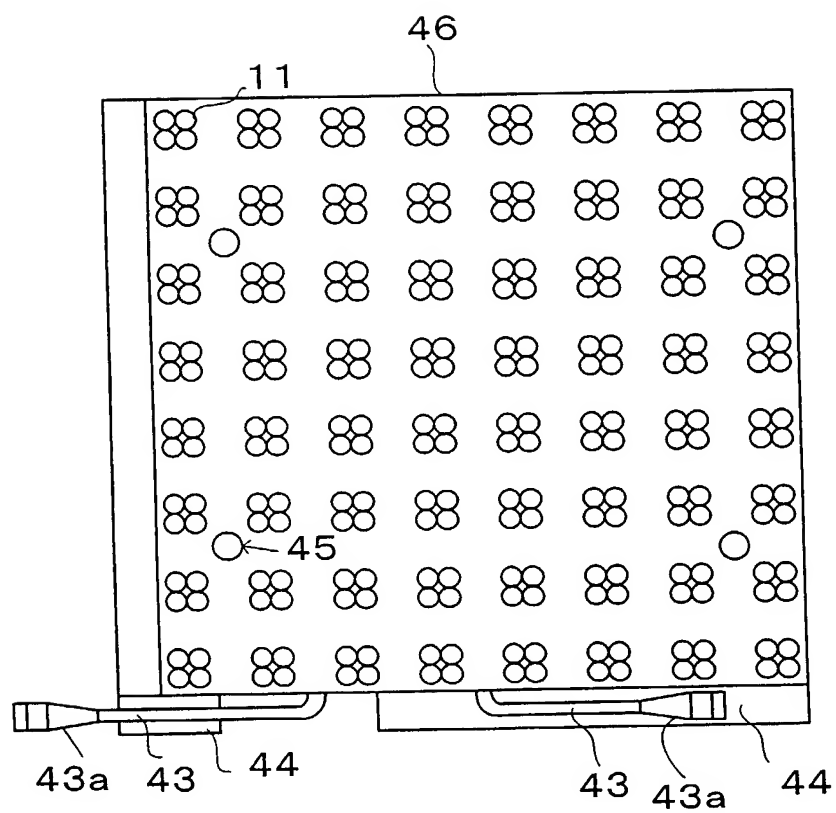


FIG. 14

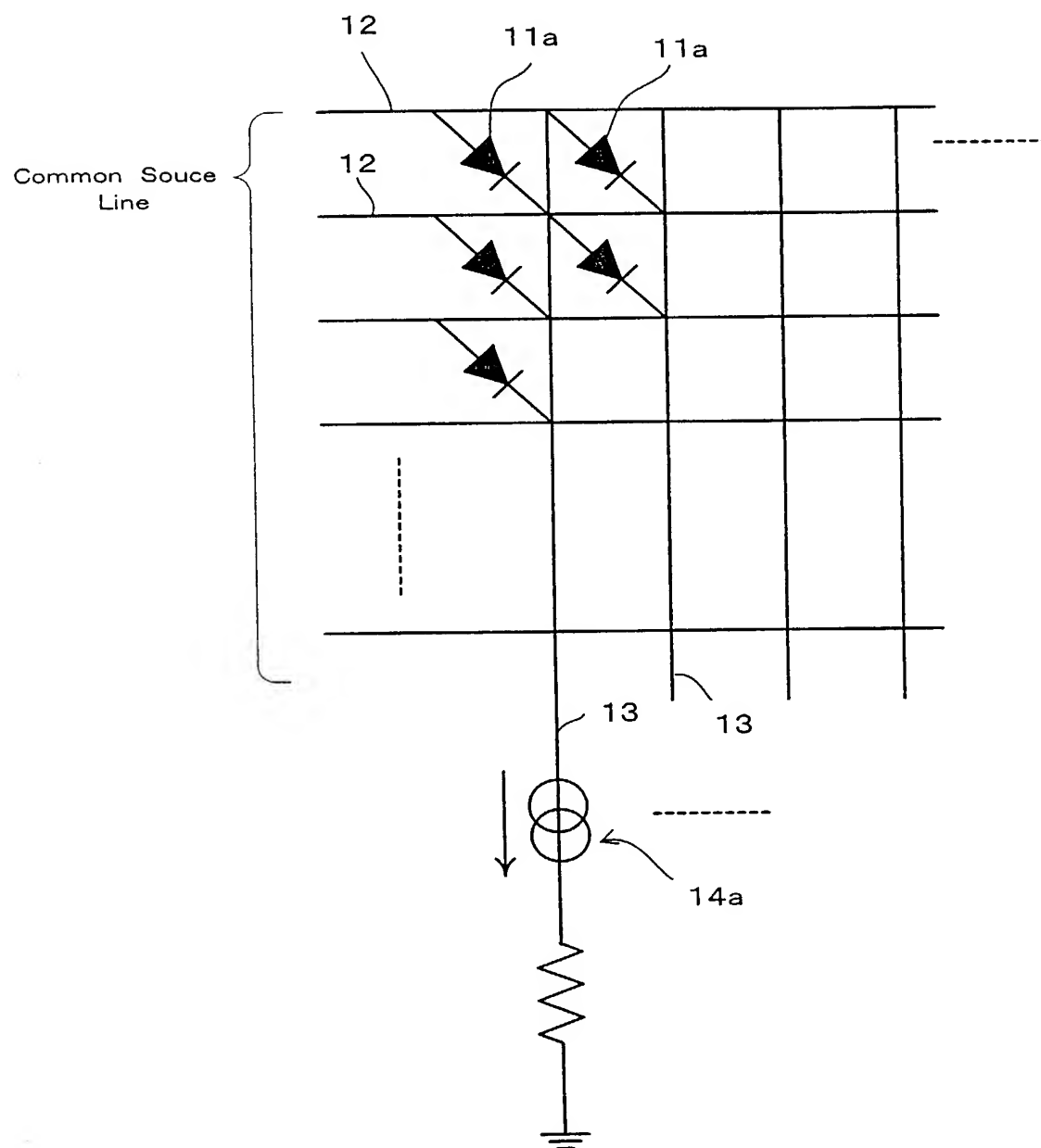


FIG. 15

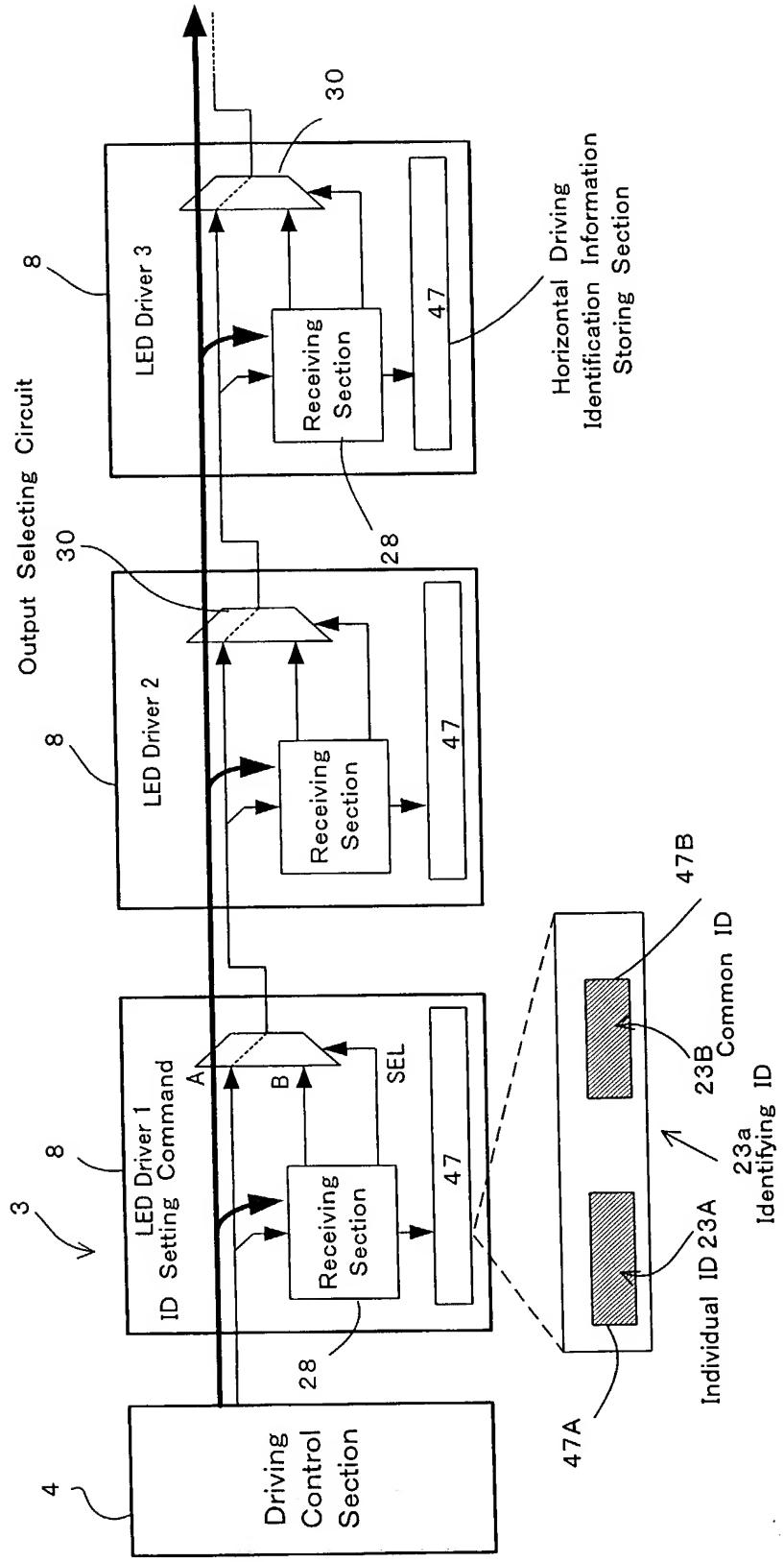


FIG. 16

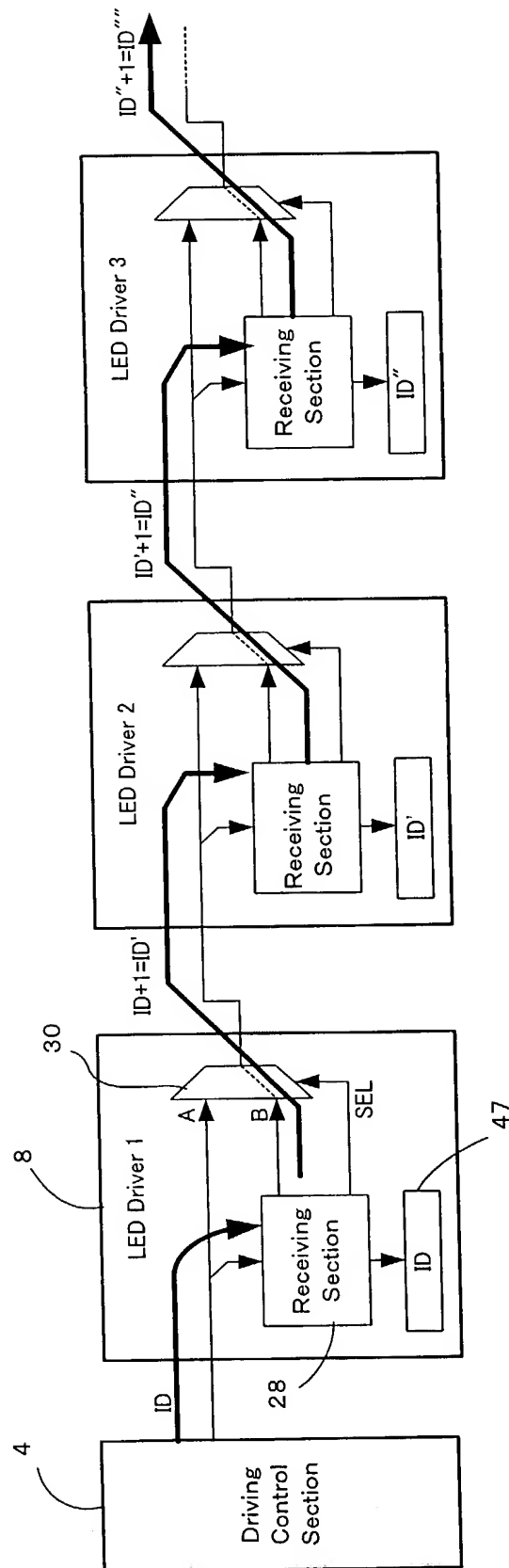
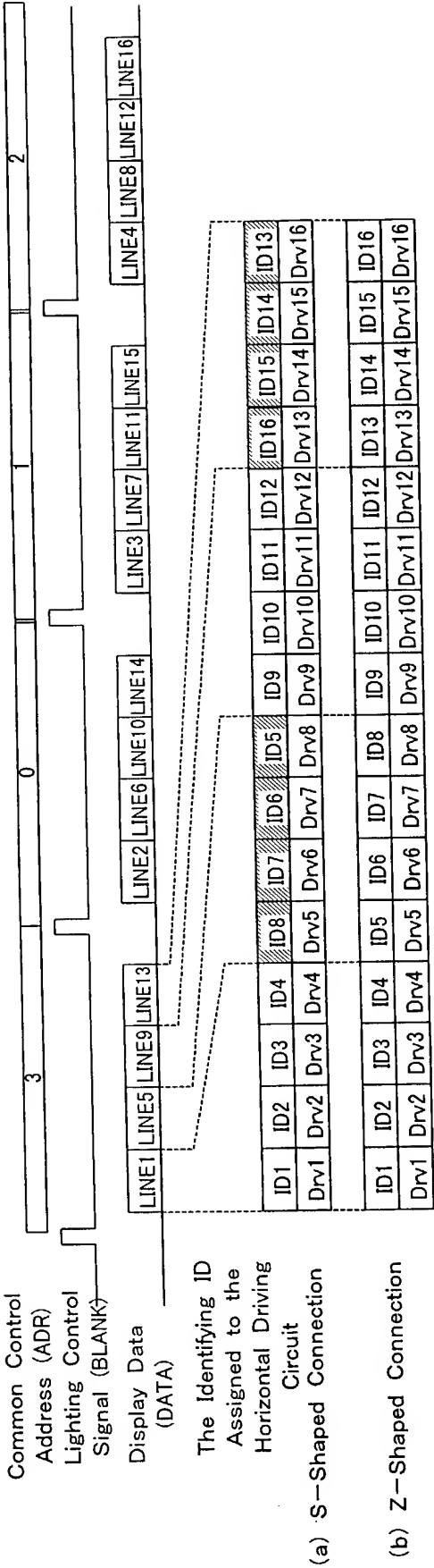






FIG. 18



10088401-072202  
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FIG. 19

(a) S-Shaped Connection (b) Z-Shaped Connection

	ID REGISTER	ID REGISTER
Driver1	ID1	ID1
Driver2	ID2	ID2
Driver3	ID3	ID3
Driver4	ID4	ID4
Driver5	ID8	ID5
Driver6	ID7	ID6
Driver7	ID6	ID7
Driver8	ID5	ID8
Driver9	ID9	ID9
Driver10	ID10	ID10
Driver11	ID11	ID11
Driver12	ID12	ID12
Driver13	ID16	ID13
Driver14	ID15	ID14
Driver15	ID14	ID15
Driver16	ID13	ID16

FIG. 20

LINE1	Pixel1	red1
LINE2	Pixel2	green1
LINE3	Pixel3	blue1
LINE4	Pixel4	
LINE5	Pixel5	
LINE6	Pixel6	
LINE7	Pixel7	
LINE8	Pixel8	
LINE9	Pixel9	
LINE10	Pixel10	
LINE11	Pixel11	
LINE12	Pixel12	
LINE13	Pixel13	
LINE14	Pixel14	
LINE15	Pixel15	
LINE16	Pixel16	

FIG. 21

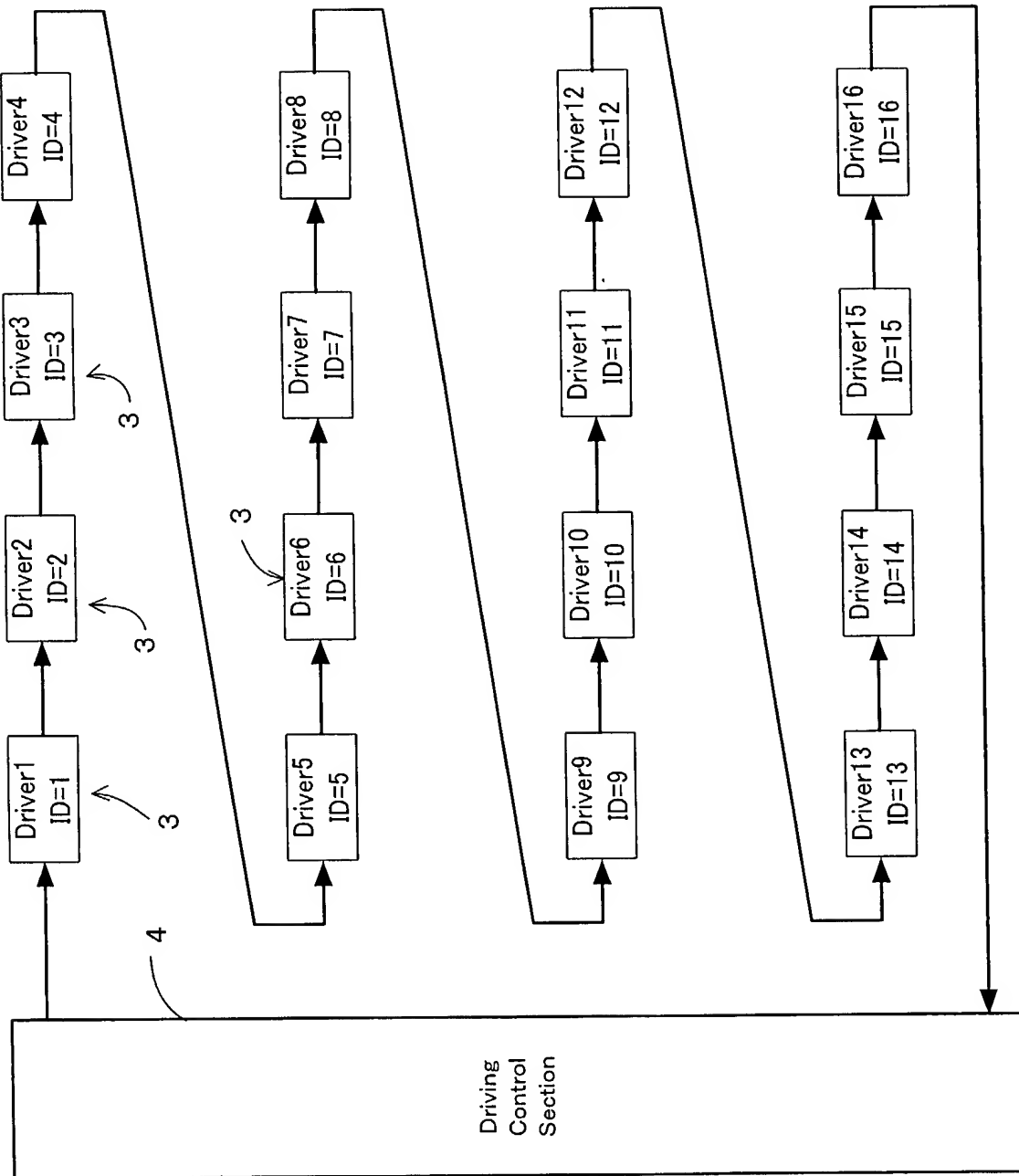


FIG. 22

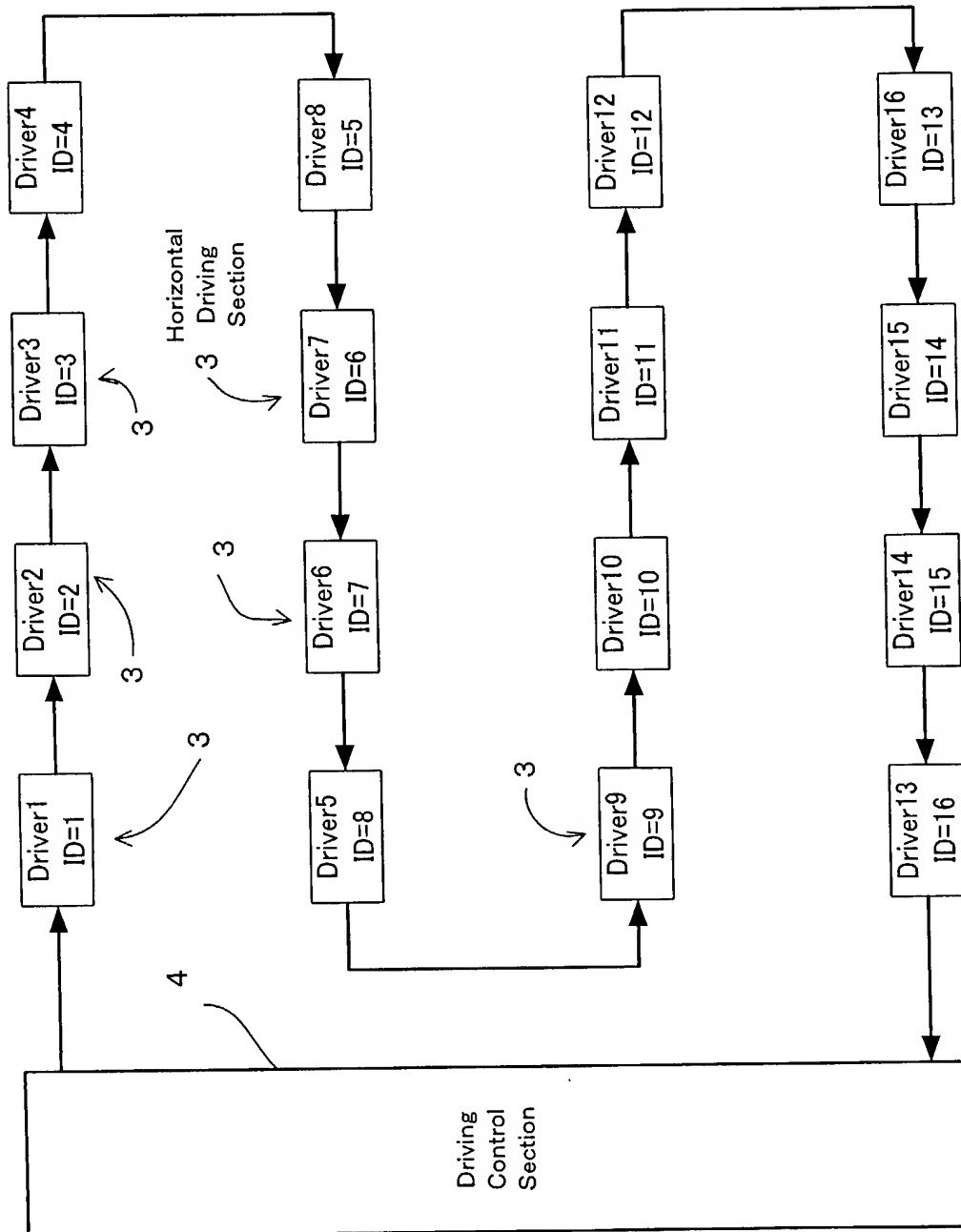


FIG. 23

